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A novel buck-boost converter

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ABSTRACT

In this paper, a novel buck-boost converter with the voltage gain of $\frac{2D-1}{1-D}$ is proposed. Output voltage is positive and the voltage stresses on the power switches and the diodes are low. Suggested topology is based on conventional boost converter. Proposed converter can provide a large step down voltage conversion ratio. Control of converter can be done with a simple I-type (Integrator) controller.

1. Introduction

Voltage bucking/boosting is required in many applications such as car electronics (Luo and Ye, 2004; Zhu and Luo, 2007a; Zhu and Luo, 2007b), fuel cell systems (Sahu and Rincón-Mora, 2004; Ren et al., 2008; Changchien et al., 2010; Liu et al., 2010) and digital devices like notebooks and cell phones. Some topologies are suggested for buck-boost converter using KY converter (Hwu and Yau, 2008; Hwu et al., 2009a; Hwu et al., 2009b). In Liao et al. (2012) a non-inverting buck-boost converter for fuel cell systems was proposed.

Ismail et al. (2008) put two switched capacitor cell into the basic converter and obtained a series of DC-DC converters but input and output are not common grounded. Miao et al. (2016) proposed a buck-boost topology with high step-down gain, common ground between input and output and low voltage stresses on switches and diodes. This paper introduces a new buck-boost converter. Suggested converter can provide a wide range of output voltages. Its control can be done with a simple I-type controller. However, its uses more switches so switching and conduction losses increase. Also, output terminal and input terminal have no common ground.

Converter's operating principles; steady-state analysis, small-signal model and controller design problem are studied in this paper. Finally, the Simulink® simulation is done.

2. Suggested topology

Suggested topology is shown in Fig. 1.

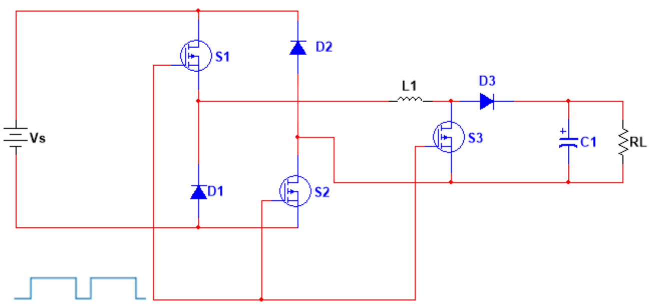

Fig. 1: Suggested topology

Switches S_1, S_2, and S_3 are turned on and off simultaneously. To derive the relationship between input and output voltages, these assumptions are made:

a) Inductor (capacitor) is very large so the current in (voltage across) it is constant.
b) Circuit is operating in steady state (i.e. voltages and currents are periodic).
c) For duty ratio of D, switches S_1, S_2 and S_3 are close for time DT and open for (1-D) T.
d) Switches and diodes are ideal.

When switches S_1, S_2 and S_3 are closed, the diodes are off and circuit is as shown in Fig. 2.

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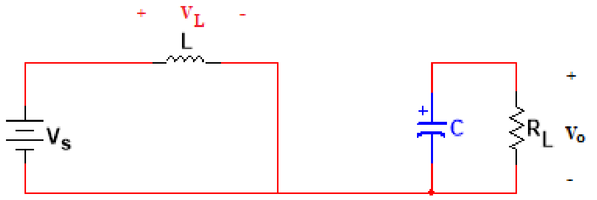

Fig. 2: Circuit with switches S_1, S_2 and S_3 closed and diodes D_1, D_2 and D_3 off

Output voltage (V_o) must be positive otherwise diode D_3 can't be reverse biased. Inductor voltage (v_L) for $0 < t < DT$ can be calculated as (Eq. 1):

$$v_L = V_s \tag{1}$$

When switches S_1, S_2 and S_3 are opened, the diodes are closed and circuit is as shown in Fig. 3.

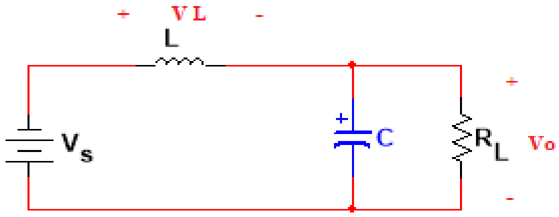

Fig. 3: Circuit with switches S_1, S_2 and S_3 opened and diodes D_1, D_2 and D_3 closed

Inductor voltage (v_L) for $DT < t < T$ can be calculated as (Eq. 2):

$$v_L = -V_s - V_o. \tag{2}$$

Average voltage across inductor must be zero for periodic operation. Eq. 1 and 2 are combined to get (Eq. 3):

$$V_s \times D \times T + (-V_s - V_o) \times (1 - D) \times T = 0 \tag{3}$$

result is (Eq. 4):

$$M = \frac{V_o}{V_s} = \frac{2D-1}{1-D}. \tag{4}$$

Voltage conversion ratio (M) vs. duty ratio (D) is shown in Fig. 4.

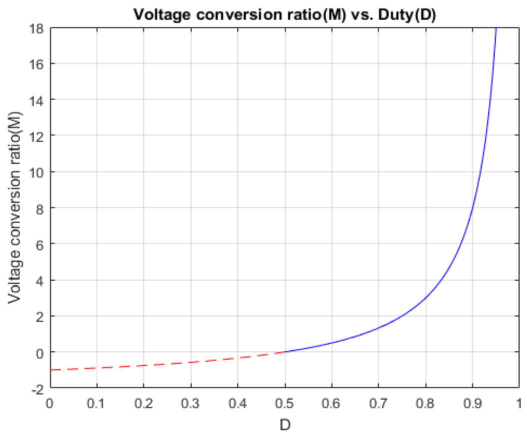

Fig. 4: Voltage conversion ratio (M) vs. duty ratio

For Continuous Current Mode (CCM) operation, the inductor current (I_L) must remain positive for all times. Maximum and minimum inductor current can be calculated as (Eqs. 5 and 6):

$$I_{L,max} = \frac{2D-1}{(1-D)^2} \times \frac{V_s}{R_L} + \frac{D}{2Lf} V_s \tag{5}$$

$$I_{L,min} = \frac{2D-1}{(1-D)^2} \times \frac{V_s}{R_L} + \frac{D}{2Lf} V_s \tag{6}$$

To determine the boundary between continuous and discontinuous current, minimum inductor current ($I_{L,min}$) is set to zero. This leads to (Eq. 7):

$$L_{min} = \frac{D}{2f} \times \frac{(1-D)^2}{2D-1} \times R_L \tag{7}$$

so, converter works in CCM if (Eq. 8):

$$L > L_{min} \tag{8}$$

3. Voltage stresses

Voltage stress on different components of the circuit is the most important criteria to choose the appropriate devices. When switches S_1,S_2 and S_3 are closed diodes D_1 and D_2 are reverse biased with voltage equal to $-V_s$ volts and D_3 is reverse biased with $-V_o$ volts. When diodes D_1, D_2 and D_3 are forward biased switches S_1, S_2 and S_3 must tolerate V_s, V_s and V_o volts, respectively.

4. Dynamic of converter

When switches S_1, S_2 and S_3 are closed ($0 < t < DT$) circuit's Eq. can be written as (Eq. 9):

$$\begin{cases} L\frac{di_L}{dt} = V_s \\ C\frac{dv_C}{dt} = -\frac{v_C}{R_L} \end{cases} \tag{9}$$

When Diodes D_1, D_2 and D_3 are forward biased ($DT < t < T$) circuit's Eq. can be written as (Eq. 10):

$$\begin{cases} L\frac{di_L}{dt} = -V_s - v_C \\ C\frac{dv_C}{dt} = i_L - \frac{v_C}{R_L} \end{cases} \tag{10}$$

Applying State Space Averaging (SSA) to these Eq. 11 leads to:

$$\begin{cases} \frac{d\tilde{i}_L}{dt} = \left(\frac{D-1}{L}\right)\tilde{v}_C + \left(\frac{2D-1}{L}\right)\tilde{v}_s + \left(\frac{V_s}{(1-D)L}\right)\tilde{d} \\ \frac{d\tilde{v}_C}{dt} = \frac{1-D}{C}\tilde{i}_L - \frac{\tilde{v}_C}{R_L C} + \frac{1-2D}{R_L C(1-D)^2}V_s\tilde{d} \end{cases} \tag{11}$$

DC Operating point can be obtained as (Eq. 12):

$$\begin{cases} I_L = \frac{2D-1}{R_L(1-D)^2} \times V_s \\ V_C = \frac{2D-1}{1-D}V_s \end{cases} \tag{12}$$

Applying Laplace transform to Eq. (11) leads to (Eq. 13):

$$\begin{bmatrix}\tilde{I}_L(s)\\ \tilde{V}_C(s)\end{bmatrix} = \begin{bmatrix} s & \frac{1-D}{L} \\ \frac{D-1}{C} & s+\frac{1}{R_LC}\end{bmatrix}^{-1} \times \begin{bmatrix}\frac{1}{(1-D)L}V_s \\ \frac{1-2D}{R_LC(1-D)^2}V_s\end{bmatrix}\times \tilde{d}(s) \qquad (13)$$

So, small signal transfer functions can be calculated as (Eq. 12):

$$\begin{bmatrix}\tilde{I}_L(s)\\ \tilde{V}_C(s)\end{bmatrix} = \frac{V_s}{s^2+\frac{1}{R_LC}s+\frac{(1-D)^2}{LC}} \times \begin{bmatrix}\left(s+\frac{1}{R_LC}\right)\frac{1}{(1-D)L}+\frac{2D-1}{R_LLC(1-D)} \\ \frac{1}{LC}+\frac{1-2D}{R_LC(1-D)^2}s\end{bmatrix}\times \tilde{d}(s) \qquad (14)$$

5. Simulation

Simulation is done for a converter with the following values:

$V_s = 100$ V, $f = 50$ Khz, $D = 0.75$, $L = 480$ μH, $C = 48$μF, $V_{On,Diode} = 0.7$ V, $r_{on,Diode} = 0.05$ Ω, $r_{MOSFET} = 40$ mΩ, $R_L = 50$.

Simulink diagram is shown in Fig. 5. Output voltage is shown in Fig. 6

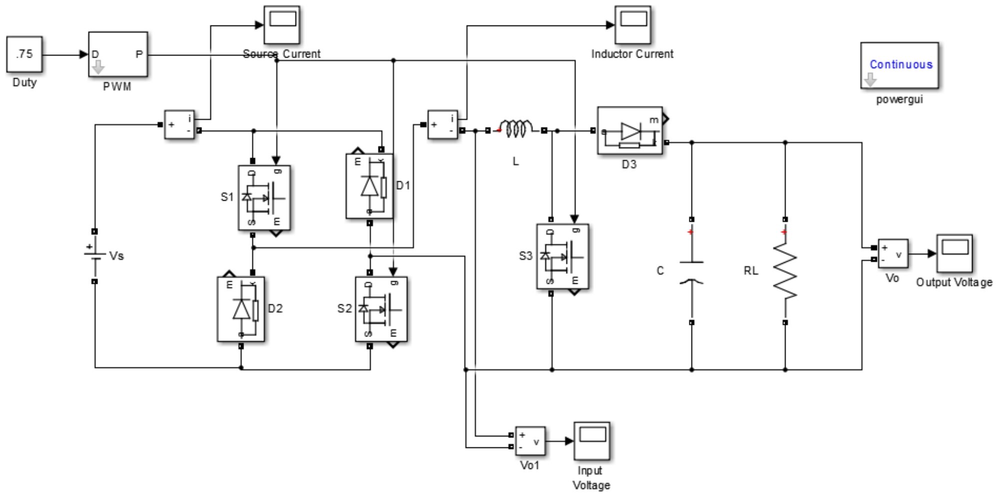

Fig. 5: Simulink diagram of proposed topology

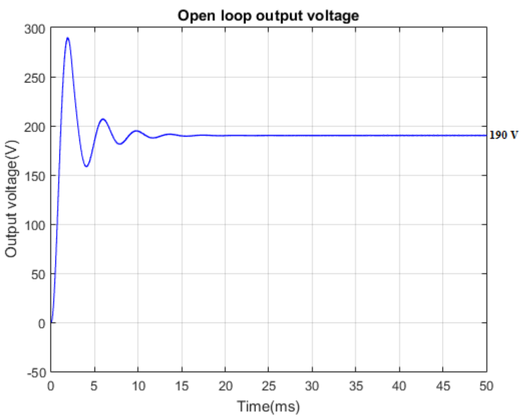

Fig. 6: Output voltage

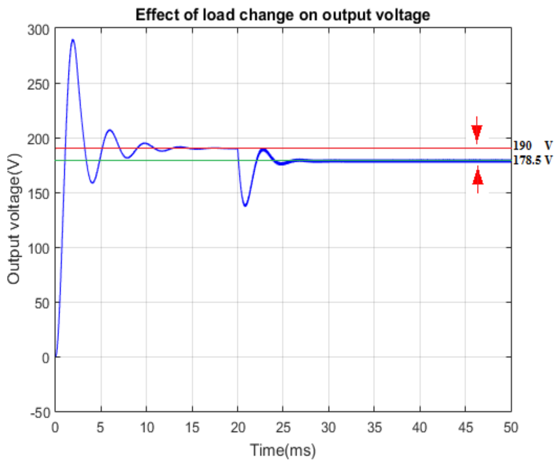

Fig.7: Effect of change in output load

Output voltage of ideal converter, i.e. converter with ideal components, must be: $\frac{2\times D-1}{1-D}\times V_s = \frac{2\times 0.75-1}{1-0.75}\times 100 = 200$ V. Output voltage of non-ideal converter is 190 V, a little less than ideal case. Assume output load changes from 50 Ω to 18.75 Ω at t= 20 ms. As shown in Fig. 7, output voltage changes.

To avoid such changes, a close loop control system must be designed. For the aforementioned values control to output transfer function is calculated as (Eq. 15):

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{-3.333\times 10^5 s+4.34\times 10^9}{s^2+416.7s+2.713\times 10^6} \qquad (15)$$

Pole-zero and Bode diagram of Eq. 15 is shown in Fig. 8 and 9, respectively.

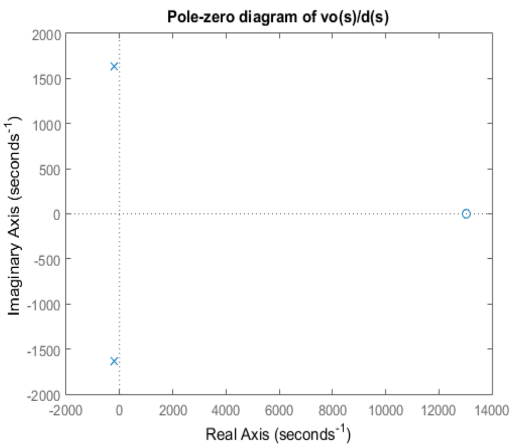

Fig. 8: Pole-zero diagram of $\frac{\tilde{v}_o(s)}{\tilde{d}(s)}$

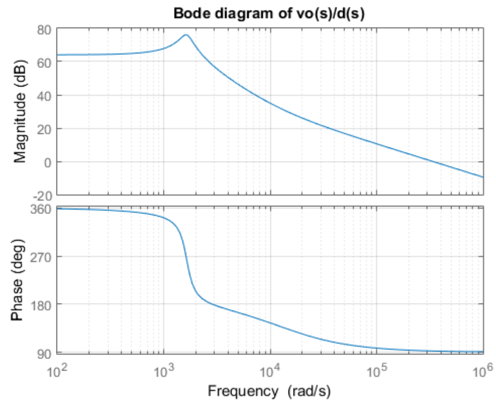

Fig. 9: Bode diagram of $\frac{\tilde{v}_o(s)}{\tilde{d}(s)}$

MATLAB provides a rich set of functions for control system analysis and design. Assume an I-type controller (Eq. 16):

$$H(s) = \frac{K_I}{s} \tag{16}$$

Using Routh-Hurwitz table $0 < K_I < 0.249$ stabilize the system. Using MATLAB's control system toolbox $K_I = 0.11$ is selected to have no overshoot. Testing the performance of close loop system is done with the aid of following scenario: Input voltage source changes from 100 V to 75 V at t=100ms, output load changes from 50 Ω to 18.75 Ω at t=200 ms and finally, control system reference signal changes form 200 V to 250 V at t= 300 ms. Table 1, summarize the aforementioned scenario.

Table 1: Test scenario

Parameter	Time	From	To	(Initial − Final)/Initial
Input voltage	100 ms	100 V	75 V	-25%
Output load	200 ms	50 Ω	18.75 Ω	-62.5 %
Reference voltage	300 ms	200 V	250 V	+25%

Response of close loop system to the test scenario is shown in Fig. 10.

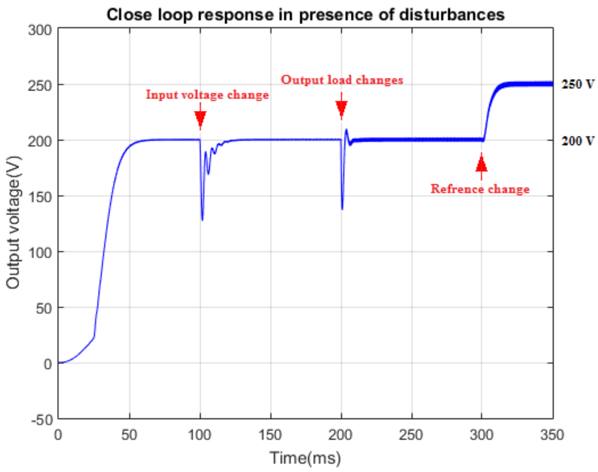

Fig. 10: Response of close loop system to load change scenario

Fig. 11 shows output voltage when reference signal of control system changes from 250 V to 5 V.

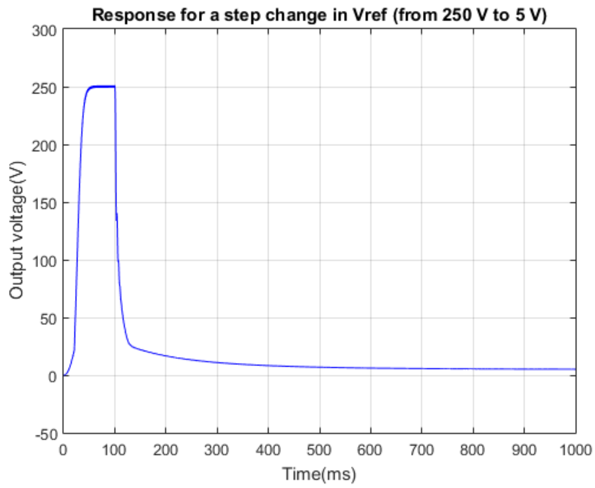

Fig. 11: Close loop response for a large change in V_{ref}

As shown in Fig. 11 proposed topology can provide a high step down gain.

6. Conclusion

Voltage bucking/boosting has many applications. A novel buck-boost topology has been proposed in this paper. Steady state, dynamical behavior and control of proposed converter has been studied. Control of suggested topology can be done with a simple I type controller. Proposed topology can provide a high step down gain and can be used for applications which load's voltage must change in a large range.

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